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Att. Docket 944-003.225
Serial No. 10/817,448

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Re application of: Matti Floman et al.

Serial 10/817,448 Examiner: Duc T. Doan

Filed: April 2, 2004 Group Art Unit: 2188

For: A FAST NON-VOLATILE RANDOM ACCESS MEMORY IN ELECTRONIC DEVICES

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BRIEF OF THE APPELLANTS

(37 CFR 1.192)

Sir:

This is an appeal from an Office Action mailed May 7, 2007, made final, in response to which a Notice of Appeal was filed on May 29, 2007. This appeal brief is being filed within one months from the mailing date of Pre-appeal Brief Conference Decision.

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Melissa L. Parise

Malissa L. Parise

Dated: December 10, 2007

For all of the reasons discussed below, it is the belief of the undersigned that the claims of the application do distinguish the invention from the art relied on by the Examiner. Nevertheless, the undersigned is always willing to discuss possible amendments to any claims to clarify or resolve any issues related to claim interpretation that may remain after the Examiner has reviewed Appellant's brief. The Examiner is strongly encouraged to call the undersigned to discuss making any such amendments.

Table of Contents

I. THE REAL PARTY IN INTEREST

The real party in interest is Nokia Corporation, having a principal place of business in Espoo, Finland.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences which are currently under consideration. The pre-appeal brief conference request was submitted on May 29, 2007 but was negatively decided on August 9, 2007 by the USPTO.

III. STATUS OF CLAIMS

Per the final Office action mailed January 11, 2007, claims 1-22, 33 and 34 are rejected. Claims 1-22, 33 and 34 are pending and are being appealed.

IV. STATUS OF AMENDMENTS

No amendments have been filed since the mailing of the final Office action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a novel methodology for a direct communication between a memory module and a processor of an electronic device (e.g., a portable electronic device, a mobile electronic device or a mobile phone) using a fast non-volatile random access memory (NVRAM) provided in that memory module. New NVRAM technologies make it possible to have a single memory unit supporting a baseband operation of an electronic device such as the mobile phone. This is possible since NVRAMs are non-volatile (no need for a separate NOR) and fast (equivalent to a DRAM speed).

According to a first aspect of the invention recited in claim 1, a memory module **25** (see Figures 1a, 1b, 2a and 2b and text on pages 8-11 of the of original patent application), comprises: a fast non-volatile random access memory **16** (also see Figure 3 and text on page 12-13 of original patent application), responsive to a command/data signal **24** provided by a processor **10**, configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said permanently stored information for providing a direct communication between said fast non-volatile random access memory **25** and the processor **10**; and a double data interface (e.g., see page 9, lines 1-2) configured to communicate with said processor **10**, wherein said memory module 25 and said processor **10** are parts of an electronic device **11** (see Figures 1a, 1b, 2a, 2b and 3 for corresponding element/module numbers).

According to a second aspect of the invention recited in claim 20, an electronic device **11** (see Figures 1a, 1b, 2a and 2b and text on pages 8-11 of the of original patent application), comprises: a processor **10**, configured to provide a command/data signal 24 and optionally for providing an overall operation control of said electronic device; a fast non-volatile random access memory **16** (also see Figure 3 and text on page 12-13 of original patent application), responsive to the command/data signal **24**, configured to provide a permanent storage of information before said command/data signal **24** is provided, configured to execute a command comprised in said command/data signal using said stored information; and a double data interface (e.g., see page 9, lines 1-2) configured to communicate with said processor **10** (see Figures 1a, 1b, 2a, 2b and 3 for corresponding element/module numbers).

The third aspect of the invention recited in claim 33 is similar to the first aspect of the present invention, as described above. The memory module **25** (see Figures 1a, 1b, 2a and 2b and text on pages 8-11 of the of original patent application), recited in claim 33 comprises: means for uninterrupted storage, which is presented, e.g., asa fast non-volatile random access memory **16** (see Figure 3 and text on page 12-13 of original patent application), responsive to a command/data signal **24** provided by a processor **10**, configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said permanently stored information for providing a direct communication between said fast non-volatile random access memory **25** and the processor **10**; and means for doubling data rate which is presented for example as a double data interface (e.g., see page 9, lines 1-2), configured to communicate with the processor **10**.

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

The following issues will be addressed in the argument:

i) whether Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) renders the invention defined by claims 1-4, 8, 12, 20-22, 33 obvious under 35 U.S.C. 103(a);

ii) whether Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 4 and further in view of Witek et al. (US Patent No. 7093153), renders the invention defined by claims 5 and 7 obvious under 35 U.S.C. 103(a);

iii) whether Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US

Patent Publication 1005/0128322 and further in view of Witek et al. (US Patent No. 7093153) as applied to claim 5 and in view of Micron (Mikron's synchroneous DRAM 256Mb: x4, x8, x16SDRAM features), renders the invention defined by claims 6 obvious under 35 U.S.C. 103(a);

iv) whether Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 1 and further in view of Pua et al. (US Patent Application No. 2005/0041473), renders the invention defined by claims 9-11, 13-18 and 34 obvious under 35 U.S.C. 103(a); and

v) whether Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 1 and further in view of Coufal et al. (IBM Technical Bulletin, Vol. 37, No. 11 November 1994, pp. 421-424), renders the invention defined by claim 19 obvious under 35 U.S.C. 103(a).

VII. GROUPING OF THE CLAIMS

Independent claims 1, 20 and 33 are argued separately.

Dependent claims 3-4, 8 and 19 stand or fall with claim 1. Dependent claims 21-22 stand or fall with claim 20.

Claims 2, 5-7, 9-18 and 34 are dependent claims (directly or indirectly) of independent claims 1 and 33, respectively, but include significant further limitations compared to claims 1 and 33 as described below, and so is believed separately patentable.

VIII. ARGUMENT

A. CLAIM 1 IS NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claim 1 is rejected under 35 USC 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent

Publication 1005/0128322) on page 3 of the Final Office Action mailed on May 7, 2007.

In regard to claim 1 of the present invention, The Examiner states:

"As in claim 1, Ganton discloses a memory module comprising: a fast nonvolatile random access memory, responsive to a command/data signal provided by a processor (Ganton's Fig 1 discloses a fast non-volatile random access memory, in which data in 115 loading into RAM #120 responsive to processor CPU using a command address data signals, see Ganton's paragraphs 11, 29; Ganton further discloses the memory #115), configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said permanently stored information (Ganton's paragraph 25 non-volatile memory provides storages for operating systems, program code, applications, radio calibration parameters and phone books information, Ganton's paragraph 30 further discloses executing using code permanently stored in the non-volatile random access memory), for providing a direct communication between said non-volatile random access memory and the processor (Ganton's Fig 1, command address/data signal providing direct communication between non-volatile memory and processor); and

Ganton does not expressly disclose a double interface configured to communicate with said processor. Ganton discloses the memory controller includes well known in the art convert circuitry to converting different protocol for interfaces with different memory devices such as non-volatile, sram, sdram etc.. Ganton further discloses using different clock edges to convert and clocking data in different memory interfaces. Ganton does not expressly disclose the double rate DDR type interface. However, Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry (Line's column 4 lines 35-39, Fig 1: #74). It would have been obvious to one of ordinary skill in the art at the time of invention to include conversion circuit and the memory storing method as suggested by Lin in Ganton's system to convert load/store commands issued by the CPU into appropriate memory access commands for accessing DDR dynamic random memory, thereby providing the system with a fast efficient method to store data into DDR DRAM in a permanent manner, see Lin's column 3 lines 57-67; Lins column 3 lines 57-62 further discloses a mechanism wherein a memory device, for example Lin's Fig 3: #68 SDRAM, readily to be a non-volatile memory by having an uninterruptible power supply (i.e. battery)),

Ganton and Lin do not expressly disclose the claim's aspect of electronic device's parts. However, Eaton discloses an electronic device (Eaton's paragraph 1, cellular phone, PDA etc..) capable of combining several parts including memory module

part (Eatons' Fig 2: #144 paragraph 15 hierarchical memory in mobile device, ROM EEPROM RAM etc..) processor part (Eaton's Fig 2: #152), speaker part (Eaton's Fig 2: #156). It would have been obvious to one of ordinary skill in the art at the time of invention to include the method of combining parts in an electronic device as suggested by Eaton in Granton's system modified by Lin which operates parts in a combination manner, thereby further providing new features while maintain the small size and portability of the electronic device (Eaton's paragraph 2).

Regarding independent claim 1, the Examiner's arguments are inaccurate and do not follow the MPEP guidelines. Thus, the Exmainer's interpretation of the quoted references needs further clarification in order to distinguish the present invention from these references.

MPEP paragraph 2143 states:

"To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Applicant's disclosure. ***In re Vaeck***, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Furthermore, according to the case law and accepted practice of the US patent office there are several criteria which should be applied in determining obviousness, where the rejection is made under 35 U.S.C. 103. These criteria based on the case law are summarized below.

1. When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the

references. ***Winner Int'.l Royalty Corp. v. Wang***, 202 F.3d 1340, 1348, 53 USPQ2d 1580, 1586 (Fed. Cir.) cert. denied, 530 U.S. 1238 (2000). In addition, court requires the Patent and Trademark Office to make specific findings on a suggestion to combine prior art references. ***In re Dembiczak***, 175 F.3d 994, 1000-01, 50 USPQ2d 1614, 1617-19 1 (Fed. Cir. 1999).

2. The Federal Circuit instructs that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).
3. The Federal Circuit reasons in ***Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc.***, 73 F.3d 1085, 1088-89, 37 USPQ2d 1237, 1239-40 (Fed. Cir. 1995), ***cert denied,*** 519 U.S. 822 (1996) that for the determination of obviousness, the court must answer whether one of ordinary skill in the art who sets out to solve the problem and who had before him in his workshop the prior art, would have been reasonably expected to use the solution that is claimed by the Applicant. However, "[o]bviousness may not be established using hindsight or in view of the teachings or suggestions of the invention." ***Para-Ordnance***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc v. Garlock Inc.,*** 721 F.2d 1540, 1548, 220 USPQ 303, 309 Fed. Cir 1983), ***cert. denied,*** 469 u.s. 851 (1984).

Moreover, in regard to motivation to combine references, The Federal Circuit Court has several times further expressly addressed the issue.

For example, *in re Geiger, supra,* it is stated, in holding that the USPTO "failed to establish a *prima facie* case of obviousness":

"Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital,* 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)."

Furthermore, Judge Newman, in her opinion in *In re Lee,* 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed Cir. 2002), repeats this fundamental principle:

"When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness."

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In reference to independent claim 1, the Examiner admitted that Ganton does not expressly disclose the double rate DDR type interface. However the Examiner is of opinion that Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry referring to Lin's column 4 lines 35-39, Fig 1: #74.

The applicant is of opinion that Lin teaches DDR (double data rate) DRAM 68 (see col. 4, lines 38-39 of Lin) which is a **volatile** memory, thus **not** teaching a double data interface between processor and a **non-volatile memory**, as recited in claim 1 of the present invention, contrary to what is alleged by the Examiner. Therefore, incorporating Lin into Ganton will **teach away** from the embodiments recited in claim 1 of the present invention.

The Examiner further stated in the Office Action of May 9, 2007 that SDRAM 68 can be readily a non-volatile memory by having

an uninterruptible power supply UPS (i.e., battery). This is technically wrong: using UPS will not convert volatile memory into non-volatile memory, because, by definition, the non-volatile memories are characterized by their ability to retain the stored data even when the power is temporarily interrupted, or when the device is left without power for indefinite periods of time as compared to the volatile memories such as SRMs and DRAMs that lose the stored information under these conditions.

Furthermore, using a battery, as suggested by the Examiner, to "convert" volatile memory into "volatile" mode of operation (obviously requiring significant electrical power for an uninterrupted performance) would contradict Examiner's own statement in regard to the reference of Eaton et al., wherein the Examiner recites a small portable electronic device such as cellular phone, PDA, etc., wherein using additional battery power for maintaining permanent "non-volatile" status of the volatile memory would not make any practical sense, therefore a person skilled in the art would not be further motivated or encouraged to incorporate Lin into Ganton to come up with the subject matter of claim 1 of the present invention.

Furthermore, Examiner's reference to Eaton et al. is also questionable and practically irrelevant to claim 1 of the present invention. Using memory with corresponding processors in portable electronic devices is well known in the art. The last clause of claim 1 recites "wherein **said memory module** and said processor are parts of an electronic device." The memory 144 of Eaton et al., quoted by the Examiner, is different from the memory module 25 (see Figures 1a, 1b, 2a, 2b) of the present invention which has much greater capabilities then the memory 144 of Eaton et al. In other words, if memory 152 of Eaton et al. would have the baseband and speed capabilities (using prior art technology) of the memory module 25 described in the present

invention, then the size of the memory 152 would be practically unacceptable to use it in a camera phone 100 of Eaton et al. (see Figure 2 of Eaton et al.). Therefore, Eaton et al. does not disclose (and irrelevant to) the limitation of claim 1 stating: "wherein **said memory module** and said processor are parts of an electronic device."

Thus, Ganton, Lin and Eaton et al. do not describe and/or teach all limitations of the independent claim 1 of the present invention and fail to meet the third criterion of MPEP paragraph 2143 quoted above.

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Furthermore, in regard to claim 1 of the present invention, the Office failed to show prima facie case of obviousness and demonstrate or provide any reasonable arguments in regard to "**suggested desirability or motivation**" or "**reasonable expectation of success**" for combining references by a person skilled in the art at the time of the invention without the benefit of hindsight (assuming **for sake of argument only** that quoted references teach or suggests all the limitations of independent claim 1), as required by MPEP paragraphs 2143 (quoted above) and 2142, and by an extensive case law on the subject quoted above.

If only for the sake of argument we assume that Ganton, Lin and Eaton et al. teach or suggest all the limitations of independent claim 1 (contrary to what is proven above), there is no **suggested desirability or motivation**, expressed explicitly, implicitly or even hinted at by Ganton, Lin or Eaton et al. or generally available to one of ordinary skill in the art to modify the reference of Lin to arrive at the subject matter of claim 1 of the present invention (as required by the MPEP Paragraph 2143 referenced above and by the case law) **without the benefit of hindsight**. (the Examiner did not proof otherwise, but the Examiner **bears a burden of**

proof as stated in MPEP Paragraph 2142.)

Moreover, in regard to claim 1 of the present invention, the Examiner alleged that a person skilled in the art at the time of invention would be motivated to incorporate the reference of Lin into Ganton (which actually will teach away from the subject matter of claim 1 as shown above) in order to provide the system with a fast efficient method to store data into DDR DRAM. For this justification the Examiner refers to col. 3, lines 57-67 of Lin wherein Lin again advocates using uninterrupted power supply 70 used for self refreshing, as discussed above, and which is irrelevant to the invention recited in claim 1.

In other words, the Examiner's reasoning (e.g., to provide the system with a fast efficient method to store data into DDR DRAM) for incorporating Lin into Ganton to arrive at the subject matter of claim 1 is practically similar to "shared advantage" approach such as achieving competitive advantage or economical advantage (which can make any invention obvious) irrelevant to the "problem to be solved" by the present invention, e.g., **providing a direct communication between a memory module and a processor of the electronic device using a fast non-volatile random access memory**.

The Manual of Patent Examining Procedure (the MPEP) clearly refers to the "problem to be solved" approach and cites a relatively recent Federal Circuit case supporting its use: "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee*, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual

First, the novelty of claims 2 and 12 is provided by a novelty and non-obviousness of claim 1 as shown above in Section VIII.A (claims 2 and 12 are dependent claims of claim 1).

Furthermore, there are even more arguments can be made regarding the Examiner's rejection of claims 2 and 12 over Ganton in view of Lin: Lin teaches DDR DRAM 68 (see col. 4, lines 38-39 of Lin) which is **volatile** memory, contrary to what is taught in claim 1 of the present invention, therefore, incorporating Lin into Ganton will **further teach away** from the invention recited in claims 2 and 12 of the present invention.

Furthermore, the applicant would like to point out that in regard to the above 103(a) rejections the Examiner did not show that the references quoted by the Examiner contain suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings to arrive at the subject matter of claims 2 and 12 of the present invention without the benefit of hindsight and did not demonstrate the reasonable expectation of success by combining the references, as required by MPEP paragraph 2143, and the case law quoted above.

D. CLAIMS 3-4, 8, 21-22 ARE NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claims 3-4, 8, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) on page 3 of the Final Office Action mailed on May 7, 2007.

Claims 3-4, 8, 21-22 are dependent claims of independent claims 1 or 20, respectively. Independent claims 1 and 20 are not unpatentable under 35 U.S.C. 103(a) over Ganton in view of Lin and in further view of Eaton et al. Since each of the dependent

claims 3-4, 8, 21-22 narrows the scope of novel and non-obvious independent claims 1 or 20, claims 1 and 20 will compel novelty of claims 3-4, 8, 21-22. Therefore, claims 3-4, 8, 21-22 are not unpatentable under 35 U.S.C. 103(a) over Ganton in view of Lin and in further view of Eaton et al.

Furthermore, the applicant would like to point out that in regard to the above 103(a) rejections the Examiner did not show that the references quoted by the Examiner contain suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to arrive at the subject matter of claims 3-4, 8, 21-22 of the present invention without the benefit of hindsight and did not demonstrate the reasonable expectation of success by combining the references, as required by MPEP paragraph 2143, and the case law quoted above.

E. CLAIMS 5 and 7 ARE NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 4, and in view of Witek et al. (US Patent No: 7093153) on page 6 of the Final Office Action mailed on May 7, 2007.

First, the novelty of claims 5 and 7 is provided by a novelty and non-obviousness of claim 4 as shown above in Section VIII.D (claims 5 and 7 are dependent, directly or indirectly, of claim 4).

Moreover, the Applicant further disagrees with the rejection of claims 5 and 7 because Witek et al. do not clearly describe unique limitations of these claims, contrary to what is alleged by the Examiner. For example, regarding claim 5, Witek

et al. talk about SRAM controller 161 which in general is a controller for volatile SRAM memory **and not a part of the non-volatile memory** as recited in claim 5 of the present invention. Therefore, combining capabilities of the SRAM controller 161 (the same is applied to the controller 162 of Witek et al.) with teaching of Ganton will teach away from the present invention of claim 5 because the controller 161 or 162 is not a part of the non-volatile memory as recited in claim 5 of the present invention.

Regarding unique limitations of claim 7, the Examiner's arguments are inaccurate because Witek et al. do not disclose all unique limitations of claim 7, contrary to what is alleged by the Examiner: Witek et al. do not talk specifically about write protection in col. 5, lines 54-63 of Witek et al., as recited in claim 7.

Furthermore, the applicant would like to point out that in regard to the above 103(a) rejections the Examiner did not show that the references quoted by the Examiner contain suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to arrive at the subject matter of claims 5 and 7 of the present invention without the benefit of hindsight and did not demonstrate the reasonable expectation of success by combining the references, as required by MPEP paragraph 2143, and the case law quoted above.

F. CLAIM 6 ARE NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 5, and in view of and in view of Micron(Mikron's synchroneous DRAM 256Mb: x4, x8,

x16SDRAM deatures) on page 7 of the Final Office Action mailed on May 7, 2007.

The novelty of claim 6 (which is a dependent claim of claim 5) is provided by a novelty and non-obviousness of claim 5 as shown above in Section VIII.D.

Furthermore, the applicant would like to point out that in regard to the above 103(a) rejection the Examiner did not show that the references quoted by the Examiner contain suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to arrive at the subject matter of claim 6 of the present invention without the benefit of hindsight and did not demonstrate the reasonable expectation of success by combining the references, as required by MPEP paragraph 2143, and the case law quoted above.

G. CLAIMS 9-11, 13-18 and 34 ARE NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claims 9-11, 13-18 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 4, and in view of Pua et al. (US Patent Application No: 2005/0041473) on page 8 of the Final Office Action mailed on May 7, 2007.

First, the novelty of dependent claims 9-11, 13-18 and 34 is provided by a novelty and non-obviousness of claims 1 and 33 as shown above in Sections VIII.A and VIII.B (claims 9-11, 13-18 and 34 are dependent claims of claims 1 and 34).

In addition, the Applicant is of opinion that Examiner's arguments are inaccurate in regard to unique limitations recited in dependent claims 9-11, 13-18 and 34. For example in claim 9, Pua et al. disclose the non-volatile memory storage integrated

findings with respect to the motivation to combine references); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). MPEP 2143.01.

Thus, based on all above arguments, claim 1 is not obvious under 35 U.S.C. 103(a) as being unpatentable over Ganton in view of Lin and in further view of Eaton et al.

B. CLAIMS 20 and 33 ARE NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claims 20 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322)) on page 3 of the Final Office Action mailed on May 7, 2007.

Claims 20 and 33 are independent claims, which are similar in scope to claim 1 of the present invention. The Examiner stated that claims 20 and 33 are rejected for the same reason as claim 1 (see Office Action of May 7, 2007, page 6). Therefore, arguments made in Section VIII.A above regarding novelty and non-obviousness of independent claim 1 are fully applied to claims 20 and 33 of the present invention. Therefore, claims 20 and 33 are not obvious and not unpatentable under 35 U.S.C. 103(a) over Ganton in view of Lin and in further view of Eaton et al. as well.

C. CLAIMS 2 AND 12 ARE NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) on page 3 of the Final Office Action mailed on May 7, 2007.

circuit 10 (see par. 20, lines 4-6) and does not contain "mass" memory which is further evident from the description of Pua et al.: "to easily extend the capacity of the non-volatile memory storage integrated circuit 10, by merely connecting the terminal corresponding to the SRAM IC 1411 to the desired memory terminal (see par 20 of Pua et al.). Claims 10-11, 13-18 are dependent claims of claim 9, so even further arguments in regard to unique limitations of claims 10-11, 13-18 not disclosed by the references quoted by the Examiner can be made, if requested by the Office.

In regard to claim 34, the Examiner's reference to the fact that Pua et al. disclose the **circuitry integrated into a module** is irrelevant to unique limitations of claim 34 of the present invention.

Furthermore, the applicant would like to point out that in regard to the above 103(a) rejections the Examiner did not show that the references quoted by the Examiner contain suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to arrive at the subject matter of claims 9-11, 13-18 and 34 of the present invention without the benefit of hindsight and did not demonstrate the reasonable expectation of success by combining the references, as required by MPEP paragraph 2143, and the case law quoted above.

H. CLAIM 19 IS NOT OBVIOUS UNDER 35 USC SECTION 103(a)

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Patent 6792499) in view of Lin (US Patent 6792499) and in further view of Eaton et al. (US Patent Publication 1005/0128322) as applied to claim 1 and further in view of Coufal et al. (IBM Technical Bulletin, Vol. 37, No. 11 November 1994, pp. 421-424) on page 11 of the Final Office

Action mailed on May 7, 2007.

The novelty of dependent claim 19 is provided by a novelty (claim 19 is dependent claim of claims 1).

Furthermore, the applicant would like to point out that in regard to the above 103(a) rejections the Examiner did not show that the references quoted by the Examiner contain suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to arrive at the subject matter of claim 19 of the present invention without the benefit of hindsight and did not demonstrate the reasonable expectation of success by combining the references, as required by MPEP paragraph 2143, and the case law quoted above.

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It is respectfully noted that the objections and rejections of the Official Action of January 11, 2007 have been shown to be inapplicable, reversal thereof is requested, and passage of the claims 1-29 to issue is solicited.

IX. CONCLUSION

For all of the aforementioned reasons, it is respectfully submitted that the rejections of all the claims in the application, namely claims 1-29, are in error, and the rejections should be reversed. Early allowance of all the claims in the application is earnestly solicited.

Respectfully submitted,

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X. APPENDIX--THE CLAIMS INVOLVED IN THE APPEAL

1. (Previously Presented) A memory module, comprising:

a fast non-volatile random access memory, responsive to a command/data signal provided by a processor, configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said permanently stored information for providing a direct communication between said fast non-volatile random access memory and the processor; and

a double data interface configured to communicate with said processor,

wherein said memory module and said processor are parts of an electronic device.

2. (Previously Presented) The memory module of claim 1, wherein said double data interface is between the processor and the fast non-volatile random access memory and is a double data rate type.

3. (Previously Presented) The memory module of claim 1, wherein the fast non-volatile random access memory is configured to provide a temporal storage of data comprised in said command/data signal.

4. (Previously Presented) The memory module of claim 3, wherein said fast non-volatile random access memory comprises:

an information storage area configured to permanently store said information; and

a temporal data storage area configured to temporally store said data.

5. (Previously Presented) The memory module of claim 4, wherein said fast non-volatile random access memory further comprises:

at least one register configured to set operating parameters of the fast non-volatile random access memory or to protect said data or said information during said execution.

6. (Previously Presented) The memory module of claim 5, wherein said operating parameters comprise at least one of of: timings for a particular frequency, and frequency ranges with a corresponding core voltage range.

7. (Previously Presented) The memory module of claim 5, wherein protecting said data or said information during said execution comprises a write protection.

8. (Previously Presented) The memory module of claim 1, wherein said information comprises an application program for operating said electronic device.

9. (Previously Presented) The memory module of claim 1, further comprising:

a mass memory, configured to provide further information in response to a command/information signal; and

an application-specific integration circuit, responsive to said command/data signal, configured to provide said command/information signal.

10. (Original) The memory module of claim 9, wherein said further information is provided to said fast non-volatile random access memory.

11. (Previously Presented) The memory module of claim 10, wherein said fast non-volatile random access memory is configured

to execute a further command comprised in said command/data signal using said further information.

12.(Previously Presented) The memory module of claim 9, wherein an interface between the application-specific integration circuit and the fast non-volatile random access memory is a double data rate type.

13.(Previously Presented) The memory module of claim 9, wherein a non-volatile random access memory-integrated circuit package contains the application-specific integration circuit, the mass memory and the fast non-volatile random access memory, or said non-volatile random access memory-integrated circuit package contains the application-specific integration circuit and the fast non-volatile random access memory, or said non-volatile random access memory-integrated circuit package contains the mass memory and the fast non-volatile random access memory.

14.(Previously Presented) The memory module of claim 9, further comprising:

a dynamic random access memory, responsive to a command/data signal, configured to provide a storage of said further information, wherein said further information is provided or partially provided to the dynamic random access memory by the mass memory in response to said command/information signal.

15.(Previously Presented) The memory module of claim 14, wherein a non-volatile random access memory-integrated circuit package contains the application-specific integration circuit, the mass memory, the fast non-volatile random access memory and the dynamic random access memory, or said non-volatile random access memory-integrated circuit package contains the application-specific integration circuit and the fast non-volatile random access memory, or said non-volatile random access memory-integrated

circuit package contains the mass memory, the dynamic random access memory and the fast non-volatile random access memory.

16.(Previously Presented) The memory module of claim 14, wherein said dynamic random access memory is configured to execute a still further command comprised in said command/data signal using said further information.

17.(Previously Presented) The memory module of claim 14, wherein said electronic device comprises:

a removable mass memory, configured to provide, in response to a further command/information signal provided by the application-specific integration circuit, still further information to the fast non-volatile random access memory, or to the dynamic random access memory, or to both the fast non-volatile random access memory and to the dynamic random access memory.

18.(Previously Presented) The memory module of claim 17, wherein said fast non-volatile random access memory or the dynamic random access memory or both the fast non-volatile random access memory and the dynamic random access memory are configured to execute a further command or a still further command or both the further command and the still further command comprised in said command/data signal using said further information or said still further information or both the further information and the still further information.

19.(Original) The memory module of claim 1, wherein said fast non-volatile random access memory is a magneto-resistive random access memory, a ferroelectric random access memory, or an Ovonics memory type.

20. (Previously Presented) An electronic device, comprising

a processor, configured to provide a command/data signal and optionally for providing an overall operation control of said electronic device;

a fast non-volatile random access memory, responsive to the command/data signal, configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said stored information; and

a double data interface configured to communicate with said processor.

21. (Previously Presented) The electronic device of claim 20, further comprising:

a power and reset block, configured to reset said processor and said fast non-volatile random access memory.

22. (Previously Presented) The memory module of claim 1, wherein said electronic device is a portable electronic device, a mobile electronic device or a mobile phone.

Claims 23-32 are cancelled

33. (Previously Presented) An apparatus, comprising:

means for uninterrupted storage, responsive to a command/data signal provided by a processor, configured to provide a permanent storage of information before said command/data signal is provided, configured to execute a command contained in said command/data signal using said permanently stored information for providing a direct communication between said means for uninterrupted storage and the processor; and

means for doubling data rate configured to communicate with said processor.

34. (Previously Presented) The apparatus of claim 33, wherein said means for uninterrupted storage is a fast non-volatile random access memory and said means for doubling data rate is a double data interface.

XI. APPENDIX--EVIDENCE

Not Applicable

XII. APPENDIX—RELATED PROCEEDINGS

Not Applicable